Notice of Allowability	Application No.	Applicant(s)	
	10/022,380	MESSMER ET AL.	
	Examiner	Art Unit	
	Nirav S Amin	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *11/30/2001*.

2. ☒ The allowed claim(s) is/are *1-12*.

3. ☒ The drawings filed on *11/30/2001* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
   1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

DETAILED ACTION

Allowable Subject Matter

Claims 1-14 allowed.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Stevens (US Patent No. 6,064,626) discloses an integrated circuit [Column 2, line 15] comprising: a system bus [Column 2, line 15], a high speed functional block [Figure 3(300)] operably linked to the system bus, a high speed clock line [Figure 3(340)] for applying a high speed clock to the high speed functional block, a peripheral bus [Column 2, line 16], a low speed functional block [Figure 3(310)] operably linked to the peripheral bus, a low speed clock line [Figure 3(360)] for applying a low speed clock to the low speed functional block. However, Stevens does not disclose a circuitry for generating a wait signal, a select line for feeding a select signal line from the peripheral bus to the low speed functional block, an enable line for applying a clock enable signal to the circuitry, a wait line for feeding the wait signal to the high speed functional block, wherein the circuitry generates the wait signal from the select line signal and the clock enable signal.

Hoffman et al (US Patent No. 6,633,994) herein after referred to as Hoffman discloses an apparatus for managing communication between buses operating at different speeds, comprising: a system bus [Figure 2(103)], a high speed functional block [Figure 2] operably linked to the system bus, a high speed clock line [Figure 2(205)] for applying a high speed clock to the high speed functional block, a peripheral

bus [Figure 2(102)], a low speed functional block [Figure 2] operably linked to the peripheral bus, a low speed clock line [Figure 2(202)] for applying a low speed clock to the low speed functional block, an enable line for applying a clock enable signal to the circuitry [Figure 2(215)]. However, Hoffman does not disclose a circuitry for generating a wait signal, a select line for feeding a select signal line from the peripheral bus to the low speed functional block, a wait line for feeding the wait signal to the high speed functional block, wherein the circuitry generates the wait signal from the select line signal and the clock enable signal.

The following is an examiner's statement of reasons for allowance:

Applicant's claimed invention distinguishes over the prior art for the following reasons. The claims are allowable over the prior art of record because none of the references, either alone or in combination, discloses or renders obvious a system on a chip comprising a system bus, a high speed functional block operably linked to the system bus, a high speed clock line for applying a high speed clock to the high speed functional block, a peripheral bus a low speed functional block operably linked to the peripheral bus, a low speed clock line for applying a low speed clock to the low speed functional block, a circuitry for generating a wait signal, a select line for feeding a select signal from the peripheral bus to the low speed functional block, an enable line for applying a clock enable signal to the circuitry, a wait line for feeding the wait signal to the high speed functional block, wherein the circuitry generates the wait signal from the select line signal and the clock enable signal.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nirav S Amin whose telephone number is (571) 272-3821. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (571) 272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NSA

THOMAS LEE
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